# CS 2734, Computer Organization II
## Spring Semester, 2002
## *Second Examination*

**(35)**

1. For this problem, you are to use a xerox of Figure 5.29 (final datapath for the *single*cycle implementation of MIPS). You should put your entire answer on that xerox, and so you need only hand in that sheet. Please write your last name and first name on the left as indicated.

   You will be tracing through the path of the **`sw`** instruction on this single-cycle model. You should use a highlighter in one color to trace the path the instruction and associated data takes through the diagram. (Do *not* show data traveling to "dead-end" components, which will eventually have no effect.) Then without using a higlighter (you may use another color of highlighter if you wish), show the *relevant* control signals. (Do *not* show control signals that serve to keep "dead-end" paths from having an effect. I have written in the inputs and outputs to and from the ALU Control for you.)

   Use the following specific instruction:

```
sw $t1, 12($t0)
```

   or in machine language form:

```
0xad2a000c                          (in hexadecimal)
101011 01000 01001 0000000000001100 (fields in binary)
    43     8     9               12 (fields in decimal)
```

   Start at the left side, showing the PC coming in, and assume this instruction is read from the Instruction Memory. Show what values are traveling along the different lines, assuming the following initial values:

   (a) **`$t0`** and **`$t1`** are registers **`8`** and **`9`** (decimal), respectively.

   (b) The contents of register **`8`** is **`64`** (decimal), and of register **`9`** is **`144`** (decimal).

   (c) The PC has value **`32`**.

   (Don't forget to handle the PC as well as the rest of the instruction.)

**(35)**

2. For this problem, you are to use a xerox of Figure 5.33. (Final datapath for the *multi*-cycle implementation of MIPS.) You will be tracing through the path of the **`beq`** instruction on this multi-cycle model. You should use several colors of highlighters to trace the paths the instruction and associated data takes through the diagram. (Or you can trace these paths using more than one diagram.) Do *not* show data traveling to "dead-end" components, which will eventually have no effect.

   For this diagram, you do *not* need to give the values of control signals.

   Below the diagram, or in some other way, carefully identify *which cycle* (or step) of handling the instruction belongs to each part of the highlighted datapath (just for data, not control). Thus you should identify *Cycle 1*, *Cycle 2*, *Cycle 3*, and perhaps *Cycle 4* and *Cycle 5* (if the instruction uses Cycles 4 and 5).

   Use the following specific instruction:

```
beq   $t2, $t5, LabelA
```

   or in machine language form:

```
0x114d0004                              (in hexadecimal)
000100 01010 01101 00000 00000 000100 (fields in binary)
     4    10    13                   4 (fields in decimal)
```

   Start at the left side, showing the PC value coming in, and assume this instruction is read from the Instruction Memory. Show what values are traveling along the different lines, assuming the following initial values:

   (a) **`$t2`** and **`$t5`** are register numbers **`10`** and **`13`** (decimal), respectively.

   (b) Assume that the contents of each of these registers is **`5234`**, so you should assume that the branch is taken.

   (c) Assume the PC has value **`20`** (decimal) initially. On the proper line, give the *final* PC value, assuming the branch is taken. Don't forget to highlight the parts related to the PC as well as the rest of the instruction. *Be sure to identify the different cycles.*

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**(10)**

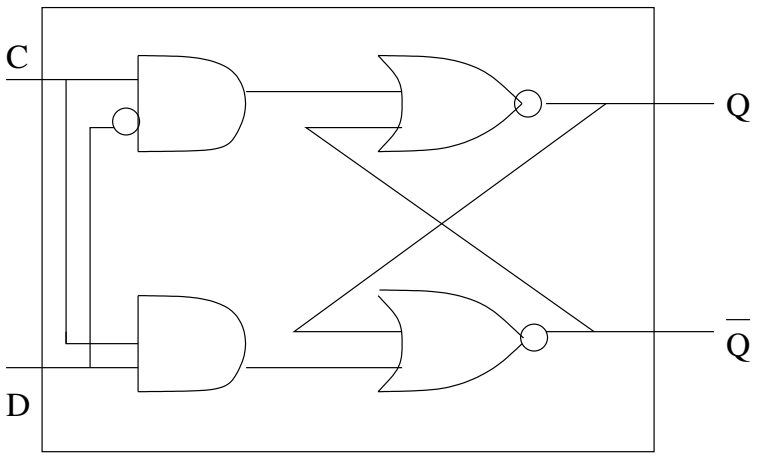
3. This question is concerned with *exceptions* and *interrupts*, as described in the text for the multi-cycle implementation.

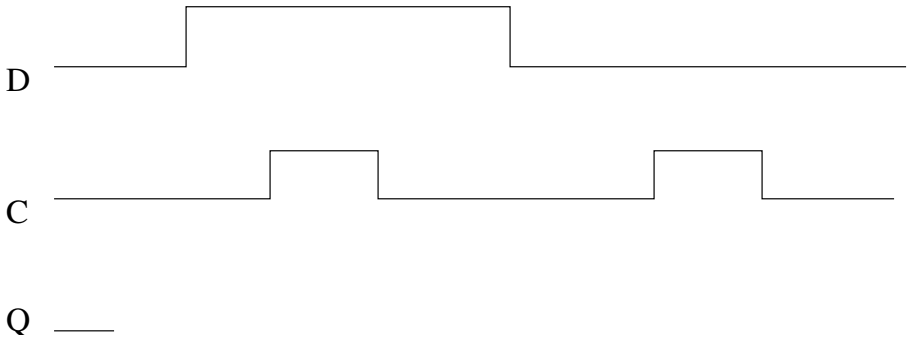
   (a) Explain very briefly how *Vectored Interrupts* work. Does MIPS use vectored interrupts? (Just "Yes" or "No.")

   (b) In case of an interrupt in MIPS because of an *undefined instruction*, what value ends up in the *EPC register*?

**(20)**

4. Consider the following diagram of a D latch from your text:




(a) Give the output Q of the D latch as it would appear in the figure above. (That is, fill in the output signal Q. Assume all three signals D, C, and Q are deasserted at first.)

(b) Explain very carefully why the output is what it is. (Your explanation should refer to the specifics of the diagram above, including the four gates.)